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Bonding with atomic rearrangement – new possibilities in material and devices technology

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In this work we present the results of investigations into direct bonding of $A^{III}B^{V}$ bulk wafers and/or epitaxial structures. A good quality junction of GaAs–GaAs, GaAs–InP, GaAs–GaP has been obtained. Bonding of GaAs/GaAlAs/GaAs epi-structures with GaAs bulk substrates enabled obtaining universal compliant substrates. On these substrates InAs epitaxial layers have been deposited. Properties of the structures have been examined by Nomarski microscopy, scanning electron microscopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM) and X-ray diffractometry.

1. Introduction

Direct bonding with atomic rearrangement is a new bonding concept in which two semiconductor wafers with free crystallographic orientation are united in thermal process without any additional adhesives [1]. It is possible to obtain in this way definite

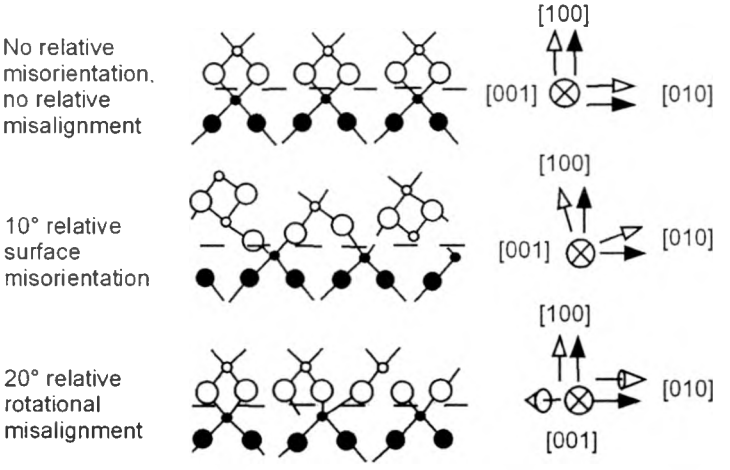


Fig. 1. Schematic diagram of the crystal structure of wafer-bonded homo-junction [1].

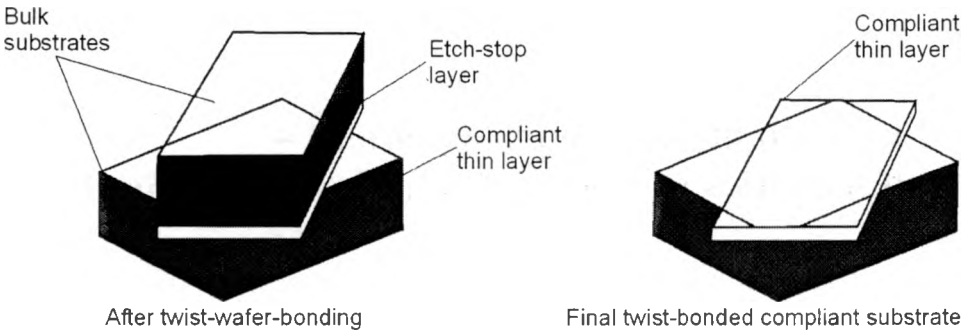


Fig. 2. Schematic processes of forming the GaAs twist-bonded compliant substrate [2].

order or disorder on the fused interface and also to integrate on one substrate devices made of free material with free orientation (Fig. 1). Another perspective application of this technique is manufacturing of universal compliant substrates for dislocation free growth of $A^{III}B^{V}$ heteroepitaxial structures [2].

A compliant substrate can be prepared by fusing very thin (~10 nm) GaAs epitaxial layer with bulk GaAs substrate (Fig. 2). Rotation of this layer with respect to the substrate provides flexibility of the compliant substrate allowing to compensate the growth strain of heteroepitaxial structures.

2. Experimental

Bonding of $A^{III}B^{V}$ bulk substrates was obtained by the method shown in Fig. 3. GaAs and InP wafers of [001] orientation and/or [111] GaP were bonded. Junctions quality was examined by the infrared microscopy, *I–V* characteristics, Nomarski microscopy, SEM and tensile failure test. For compliant substrates polished [001] GaAs wafers of

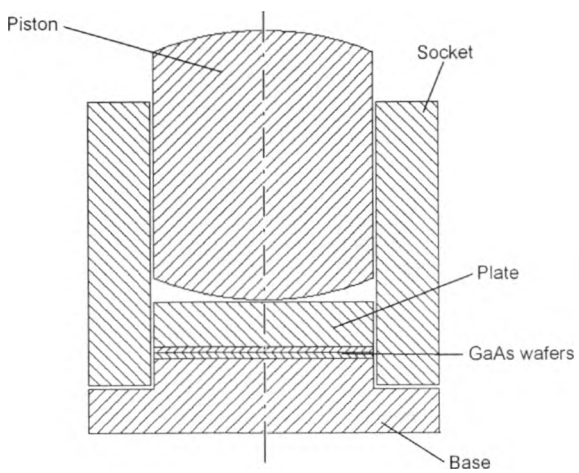


Fig. 3. Graphite apparatus for bonding of $A^{III}B^{V}$ wafers.

2" in diameter, were prepared and selected according to special procedure. Only the substrates with high surface purity and high geometrical quality (bow, total thickness variation – TTV) were used. On the native substrates, chemical etching-stop layer with thickness ~1 μm (AlAs or AlGaAs) and GaAs layer with thickness 10–1000 nm were deposited by metal-organic chemical vapour deposition (MOCVD) method. They were next fused with the host substrates in H_2 atmosphere at ~630 °C under the pressure of ~5 kG/cm^2. The native GaAs substrate was then removed by etching in H_2O_2:NH_4OH etchant. The AlGaAs layer was removed by etching in 10% HF and as a result GaAs/GaAs compliant substrates were obtained. The chemical etching is a crucial operation in obtaining the GaAs/GaAs compliant substrates. It needs the etchants with high (~6 μm/min) and low etching speed (~0.3 μm/min) and some methods for the process assessment.

Compliant substrates obtained in this work were tested by heteroepitaxial growth of InAs layers. They were also investigated by Nomarski microscope, SEM, TEM, AFM, and X-ray diffractometry.

3. Results and discussion

SEM images of GaAs–GaAs, GaAs–InP and GaAs–GaP bonded bulk wafers are shown in Fig. 4. There are no defects and inhomogeneities on the interface. Some differences in relief result from misorientation or rotation. Proper junctions were also obtained in epitaxial GaAs/AlGaAs/GaAs structures fused with host GaAs substrates (Fig. 5). SEM observations of bonded structures were very useful for controlling the wet chemical etching used to remove the native GaAs substrates and AlGaAs layers (Fig. 6). It allowed to establish the conditions for very precise etching when thin GaAs compliant layer was revealed. In Figure 7, there are SEM images of 100 nm twist bonded ($\alpha = 30°$) GaAs epilayer fused to the host substrate. "Wave shape" on the compliant surface is similar to this observed on as grown GaAs epilayer before bonding. The observations by SEM were limited up to 100 nm in thickness of bonded layer. Measurements of thinner layers (10–50 nm) were taken by AFM. AFM image of the surface of a compliant substrate and its cross-sectional analysis is shown in

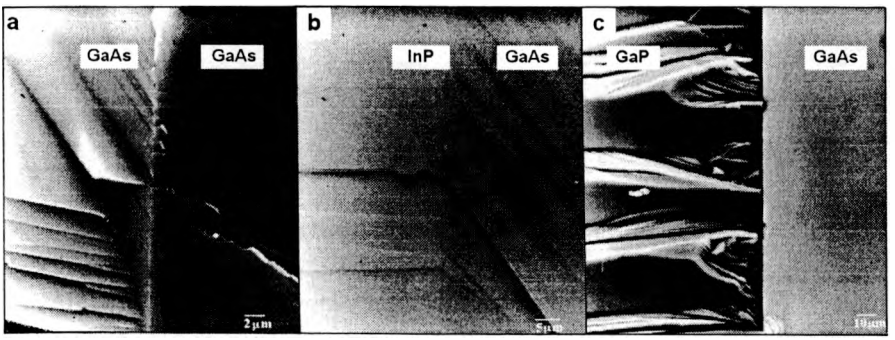


Fig. 4. SEM image of twist bonded $A^{III}B^{V}$ wafers: GaAs–GaAs (**a**), GaAs–InP (**b**), GaAs–GaP (**c**).

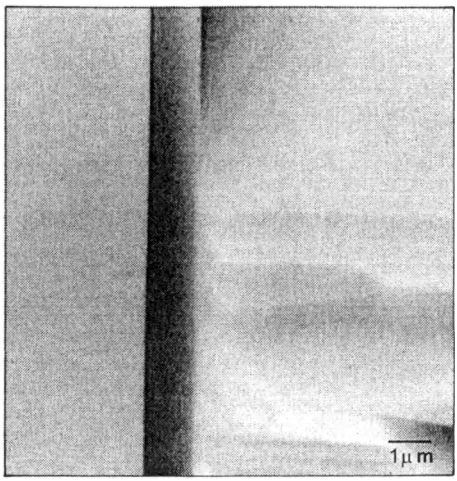
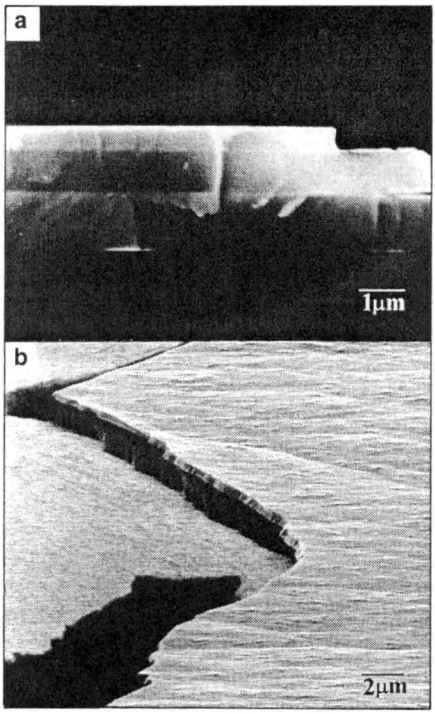


Fig. 5. SEM image of twist bonded GaAs epilayer fused to host substrate.



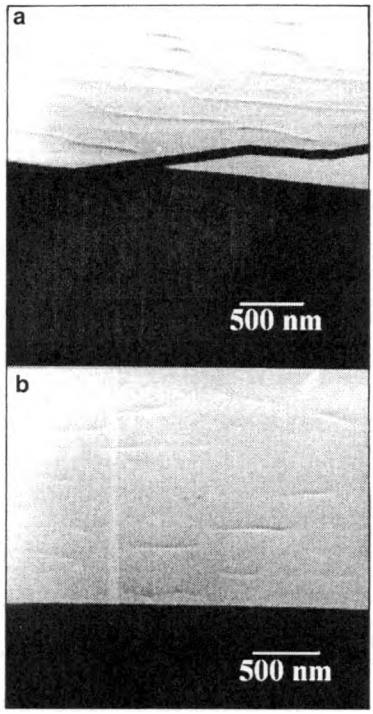


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Fig. 6. SEM image of twist bonded GaAs epilayer with partially removed native substrate: cross-section (**a**), surface (**b**).

Fig. 7. SEM image of twist bonded 100 nm GaAs epilayer fused to host substrate: relief on the "as grown" surface of GaAs epilayer (**a**), view on the compliant GaAs layer (**b**). Characteristic relief is seen.

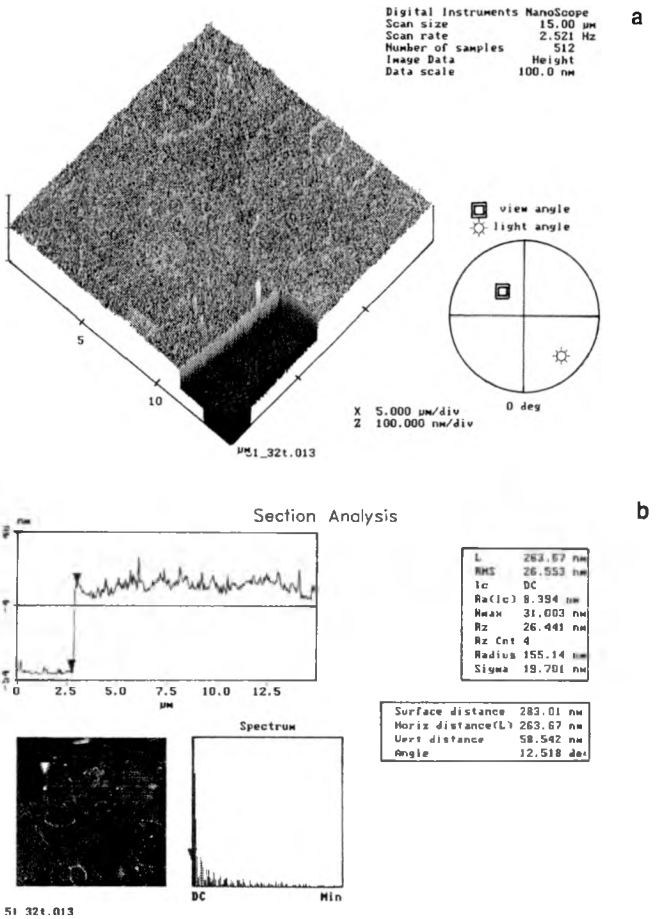

Fig. 8. AFM image of compliant substrate (**a**), and AFM cross-sectional analysis (**b**).

Fig. 8**a**, **b**. The thickness of this layer was ~50 nm. The surface quality was high and measured roughness amounted to ~0.3 nm. The heteroepitaxial MOCVD growth of InAs layers was performed on the compliant substrates of 10–50 nm thickness. This process required some modification compared to heteroepitaxy on conventional GaAs bulk substrates. A standard procedure of the heteroepitaxial growth begins with substrate annealing at ~800 °C to allow a surface structure reconstruction. At this temperature a strong decomposition of the compliant substrate was observed. The AFM images of the compliant substrate before and after annealing at 625–800 °C are shown in Figs. 9 and 10. A strong surface decomposition is observed on the substrate surface annealed at 800 °C, while at 625 °C only small decomposition occurs. Surface decomposition was not observed at temperatures below 500 °C. Taking into consideration the decomposition of the compliant substrate and critical temperature of monocrystalline MOCVD growth of InAs layer, the optimal temperature 625 °C for

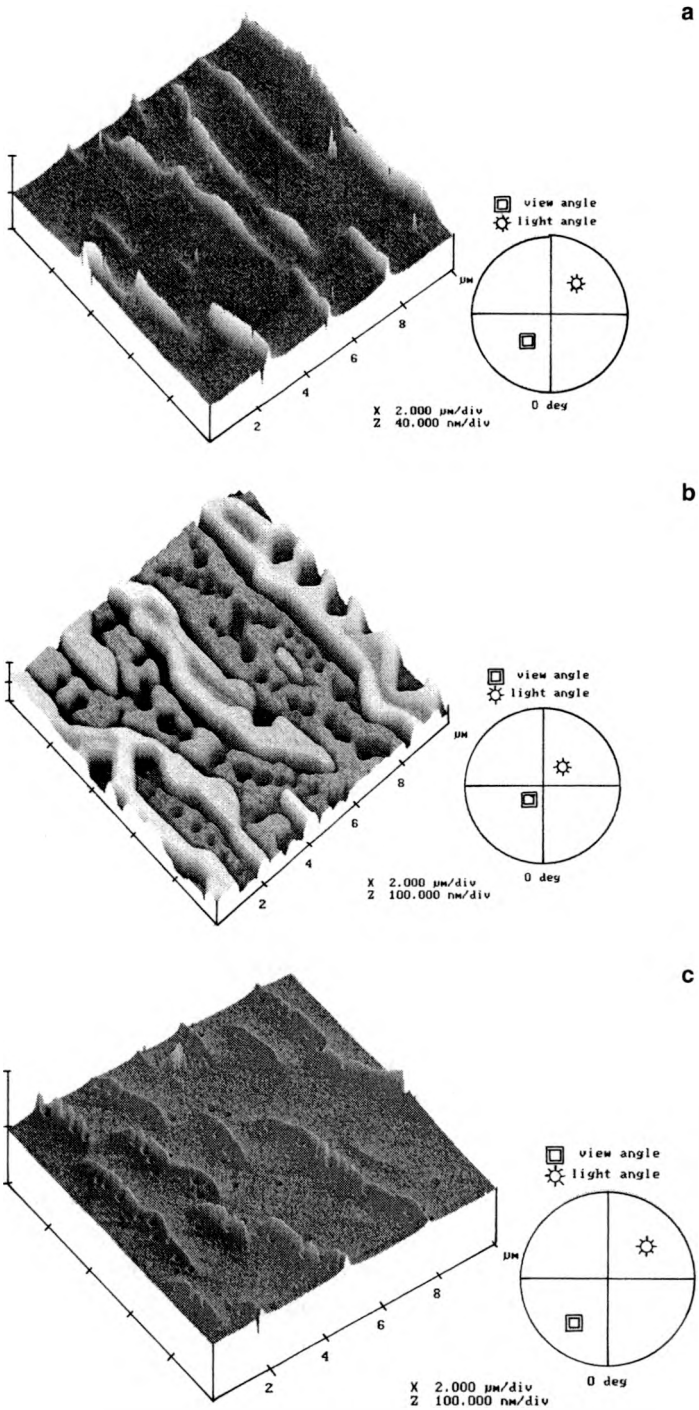

Fig. 9. AFM images of compliant substrate: before annealing (**a**), after annealing at 800 °C (**b**), after annealing at 625 °C (**c**).

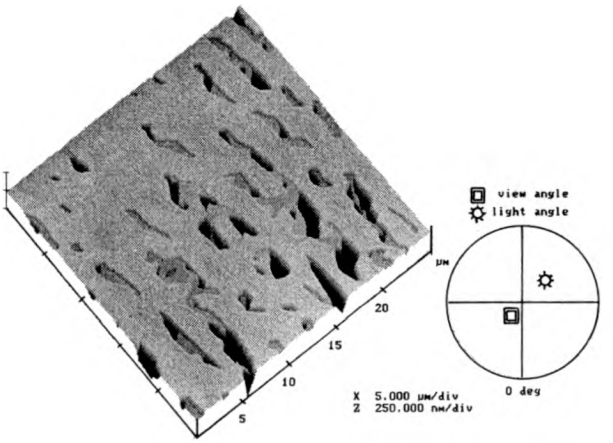

Fig. 10. AFM image of GaAs layer grown on GaAs compliant substrate annealed at 800 °C.

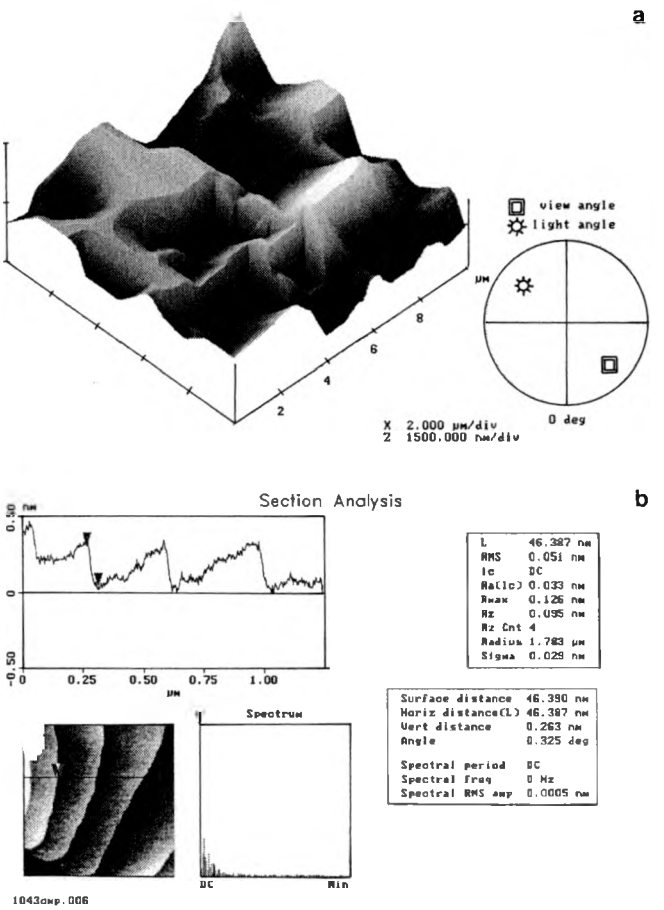

Fig. 11. AFM images of InAs layer grown on GaAs compliant substrate: morphology (**a**), atomic steps (**b**).

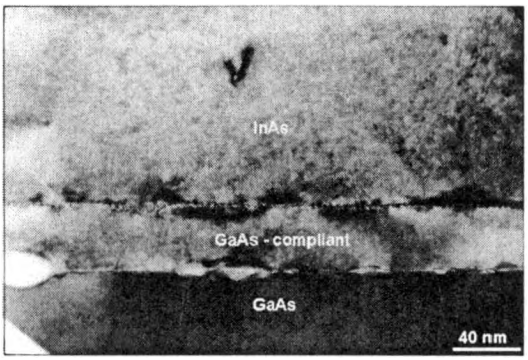

Fig. 12. Cross-sectional TEM image showing InAs film grown on GaAs compliant substrate.

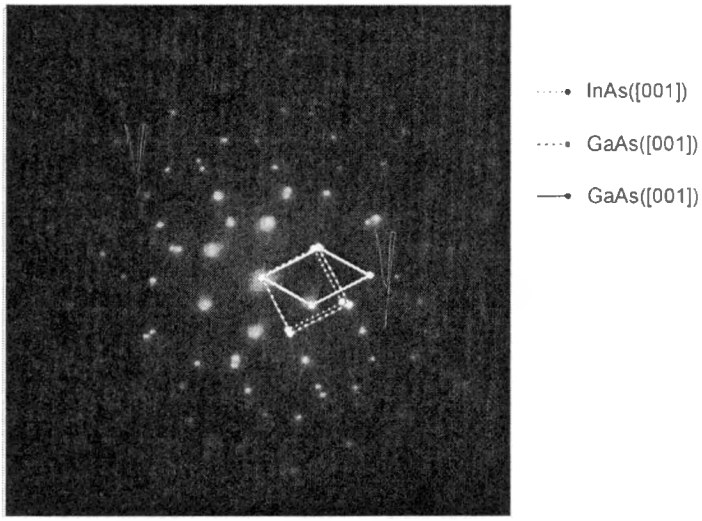

Fig. 13. Electron diffraction image of InAs layer grown on GaAs compliant substrate.

InAs/GaAs heteroepitaxial process was chosen. At this temperature InAs layers ~2 μm were deposited on GaAs compliant substrate (Fig. 11). On the surface of this layer the flat regions with atomic steps of few hundreds nanometers width were observed. This value is much greater than for layers grown on conventional substrates. In these regions we did not observed any disorders of atomic steps connected with the presence of dislocations. The InAs layers were also investigated by means of TEM. The existence of the compliant substrate was also confirmed by this method (Fig. 12). The electron diffraction image of a perpendicular cross-section of InAs/GaAs compliant substrate is presented in Fig. 13. In the picture the "elementary cells" of three two-dimensional lattices are marked. The "elementary cells" suitable for both GaAs phases (bulk substrate and compliant layer) are of the same dimensions but of different shape associated with 45° rotation of the layer with respect to the bulk substrate. The epilayer InAs shows the same orientation as GaAs compliant substrate, but its lattice constant

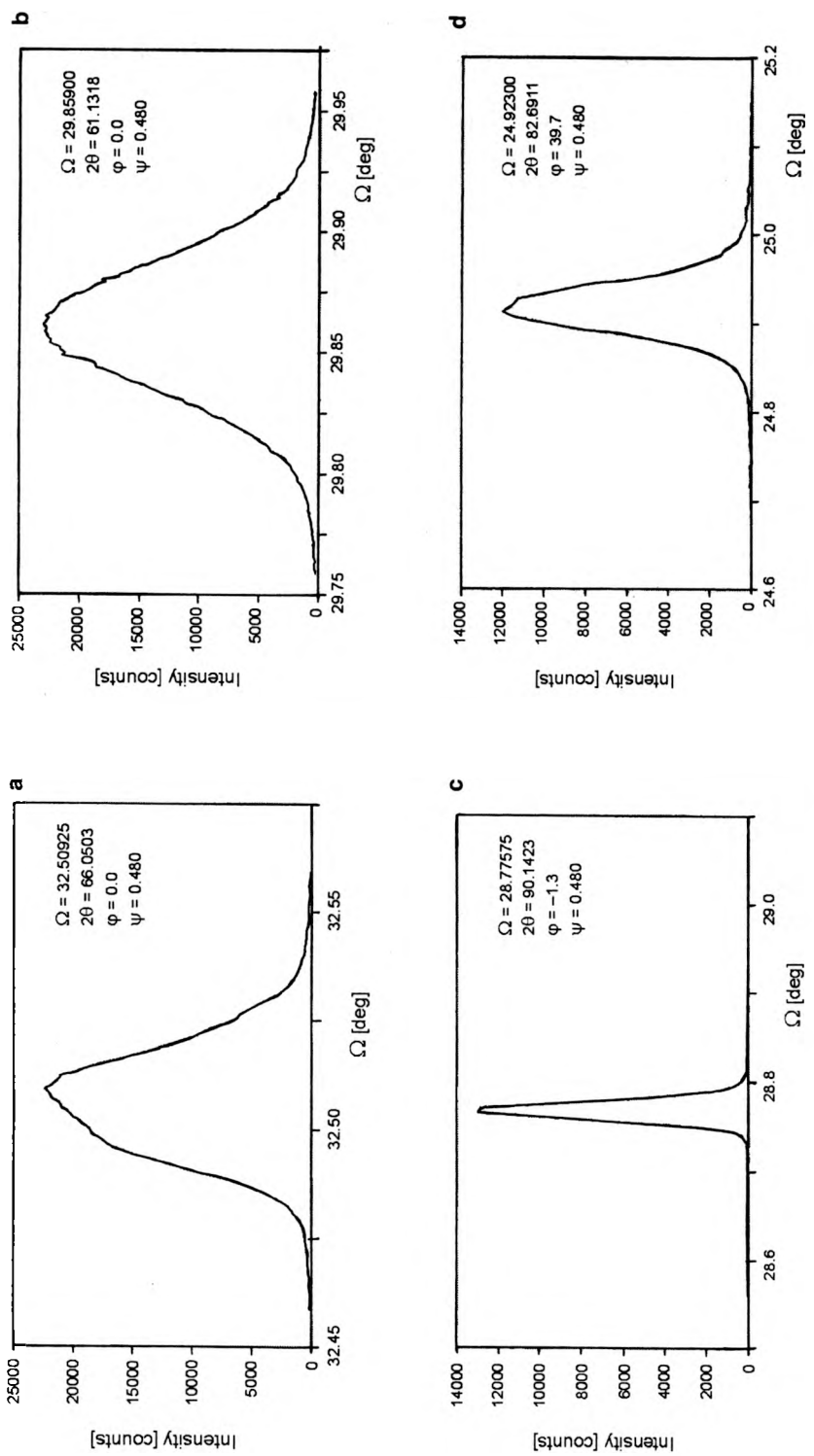

Fig. 14. X-ray diffraction curve for symmetrical [004] and asymmetrical [115] reflexes InAs layer grown on compliant substrate: reflex [004] for GaAs substrate (**a**), for InAs layer (**b**), reflex [115] for GaAs substrate (**c**), for InAs layer (**d**). Note: measurements (**c**) and (**d**) were made for different azimuthal angles φ.

is larger (elementary cell is of the same shape, but smaller in size). For further evaluation of InAs/GaAs-compliant structure X-ray diffraction method was also applied.

The reciprocal space mapping was performed around [004] and [115] reciprocal lattice points. In particular, the investigation of asymmetrical [115] reflections enabled the measurement of relative rotation of the crystal lattice in the deposited layer with respect to the crystal lattice in the substrate. The X-ray rocking curves for symmetrical [004] and asymmetrical [115] reflections for InAs/GaAs-compliant substrates are shown in Fig. 14. The evaluated value of twist angle is 42°. A similar value of twist angle was obtained from the investigation of electron diffraction (Fig. 13). For InAs layer deposited on standard GaAs substrate, the orientation of the layer was the same as that of the substrate.

4. Summary

Results of our investigations can be sumarized in the following way:

– Good quality junctions were obtained by direct bonding of GaAs–GaAs, GaAs–InP, GaAs–GaP bulk substrates.

– Compliant substrates of 10–100 nm thickness were obtained by bonding with atomic rearrangement.

– InAs epilayers were deposited on compliant substrates. The procedure of epitaxy on these substrates was different from the standard one (lower temperature) due to surface decomposition higher than that for conventional GaAs bulk substrates.

– Methods which were applied in this work were very useful in examining the used material on each step of the compliant substrate manufacturing.

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