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Transistors today – after 50 years in microelectronics

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The current status and future trends in bipolar junction transistors (BJT) and field effect transistors (FET) construction design, technology and applications are presented. The development of heterojunction bipolar transistor (HBT) and high electron mobility transistor (HEMT) devices which find a widespread use in communication and optoelectronic circuits has been closely tied with advances in epitaxial growth of semiconductor nanolayers and the so-called bandgap engineering. Application of new semiconductor materials such as SiGe, AlInAs, GaN, AlGaN in traditional devices allows improving substantially their parameters. The comparison of the performance of advanced devices is given. Research results on advanced GaN HFET (heterostructure field effect transistor) devices fabricated in our semiconductor device laboratory are presented. Future trends in the device design market are signalised.

1. Introduction

It is over 50 years now, since William Shockley patented his transresistance point contact germanium device, the first bipolar junction transistor, which brought him, together with John Bardeen and Walter Brattain, a Nobel Prize in 1956. Germanium as a basic semiconductor material has been quickly abandoned, giving way to silicon, which started to dominate in microelectronics along with an advent of monolithic circuit integration (Jack Kilby and Robert Noyce in 1958, the Nobel for Jack Kilby in 2000) in the 1960s. Silicon holds its strong position in the semiconductor market today. There are plenty of reasons for that, to name a few: near perfect crystal quality of silicon wafers and thus well predicted and described physical phenomena occurring in Si devices, good thermal and mechanical parameters, native and easy to grow insulating oxide (SiO_2) and last, but not least, the availability of the material. On the silicon basis reliable MOSFET (metal-oxide semiconductor FET) devices were implemented and gave impetus for NMOS (n-channel MOS) and CMOS (complementary MOS) digital circuits technologies, which dominate the integrated circuit (IC) market today.

On the road to higher operating frequencies a bipolar transistor has been quickly modified from a simple carrier diffusion device to a much faster drift mechanism

device and finally to a heterojunction bipolar transistor (HBT). Herbert Kroemer (Nobel Prize in 2000) did many inventions in the above development giving a detailed description of a heterostructure transistor in 1957. He continued in the field of III–V materials and high electron mobility FETs (HEMTs), which along with HBTs constitute a base for present radio frequency (RF) and optoelectronic circuits. Today's advanced InGaAs/AlGaAs/InP HEMTs reach cut-off frequencies of 300 GHz and SiGe HBTs allow design of high performance BiCMOS (bipolar-complementary MOS) digital and mixed-signal circuits operating in GHz range.

That tremendous progress would not have been possible without the development of new materials and epitaxial crystal growth using advanced instrumentation and technologies. It allowed for semiconductor heterostructure fabrication in nanoscale and bandgap engineering to create new devices. Although silicon remains a basic semiconductor for device and IC fabrication, a new SiGe alloy is finding a widespread application in high frequency bipolar devices. Group III–V semiconductors, which originated from GaAs and InP materials, now include ternary and quaternary compounds including AlInAs, GaAsSb, GaInP, GaInAsN, to name a few. A new wide bandgap material, GaN, widely used in optoelectronics, now is being introduced into high temperature and power device market. Some results concerning GaN HFET, designed and fabricated in our Semiconductor Device Laboratory are included in the paper. Current trends in material development are related to antimonide based materials, such as InAs, GaSb, AlSb that are characterised by extremely high carrier mobility and matched crystal lattice constant. Future trends in device design concentrated on organic and magnetic materials are also briefly discussed.

2. Silicon based devices

Present silicon bipolar technology evolved from the well known epi-planar technology developed in the 1970s with double diffusion processing to form the base and emitter regions. The main improvement in the structure design was shrinking the base width by ion implantation doping and use of polysilicon to form the emitter region. That allowed to rise the cut-off frequency f_T by carrier transit time reduction and to increase the current gain of the device due to the reduction in the hole component of the emitter current injected to the base. In addition to lateral, the vertical scaling is needed to minimise parasitic resistances and capacitances. The emitter width has shrunk down to 0.15 μm, which means by a factor of ten, during the last decade [1], [2]. The excellent performance of Si transistors was obtained when a double polysilicon design to form both the emitter and the base external regions had been developed. Polysilicon was deposited onto the Si wafers by the low-pressure chemical vapour deposition (LPCVD) technique. This allowed low temperature processing and self-aligning of the transistor structure regions. In the advanced design (Phillips) the resulting cut-off frequency of 20 GHz at 3 V-supply voltage and the noise factor of 1.2 dB at 2 GHz were obtained. Such performance, however, requires scaling down to 0.1 μm of the emitter width and to 100 nm of the base width along with the selectively implanted sub-collector region

and using special isolation methods [3]. Self-aligned double polysilicon transistor with implanted base and LOCOS isolation is used by many IC's manufacturers today in their bipolar and BiCMOS chips [4].

The recent decade breakthrough in bipolar transistor development came when the manufacturability of Si:Ge technology had been demonstrated. Advanced techniques of ultra-high vacuum/vapour phase epitaxy (UHV/VPE), molecular beam epitaxy (MBE) or metalorganic chemical vapour deposition (MOCVD) to grow the SiGe epitaxial alloy base was used. This resulted in graded energy gap of the base and in a large build-in electric field obtained independently of the base doping profile. The true drift transistor proposed earlier by Kroemer became a reality. A lot of inventions in the development of SiGe HBT came from IBM, where the research was driven by the need to fabricate $f_T > 60$ GHz digital circuits for a new generation of mainframe computers. In result, several designs of HBTs for bipolar and BiCMOS chips were introduced, *e.g.*, 3.3 V supply – 0.5 μm, 0.25 μm and just recently (in 2001) 0.13 μm BiCMOS technology [5], [6]. An example of HBT design is shown in Fig. 1. The state-of-the-art SiGe HBTs now allows reaching f_T above 100 GHz and f_{max} of

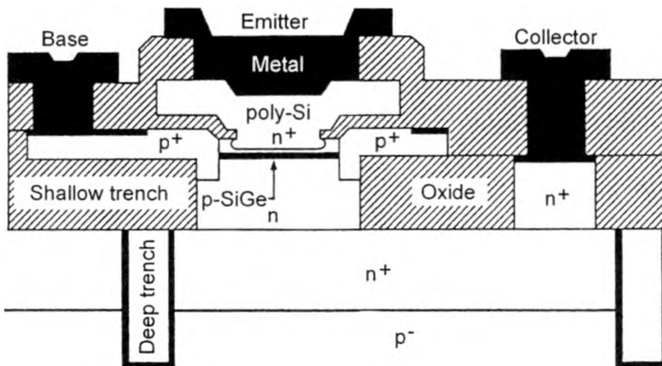

Fig. 1. Schematic cross-section of the SiGe HBT (IBM) [6].

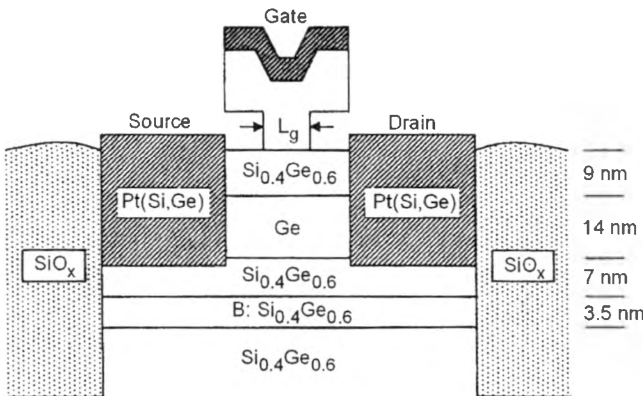

Fig. 2. Schematic cross-section of SiGe HEMT [7].

150 GHz. The inherent assets of these devices are relatively low costs of fabrication, easy implementation in Si VLSI (very large scale of fabrication) circuits, low noise factor. There are some deficiencies in the resulting parameters, *e.g.*: low breakdown voltages (3–7 V) that limit the supply voltage, poor linearity and power added efficiency. In general, SiGe HBT are better for digital circuit application where the switching action is essential; for analog circuits with the highest operating frequencies and high gain, III–V compound HBTs are the solution.

There are also reports on SiGe HEMT (MODFET – modulation doped FET) devices, which take advantage of high carrier mobility in germanium quantum well and the strained SiGe lattice [7]. An example of the design is shown in Fig. 2. The reported value of f_T was 42 GHz.

3. III–V compound devices

The III–V HBTs are usually based on InP substrates and are at present the fastest transistors available. Using GaInAs for the base material and AlInAs for the emitter region a high valence band offset at the emitter-base junction is obtained. The ternary compounds have usually composition required for lattice-match to InP substrate. Recently, another ternary compound such as GaAsSb was used for the base. It has higher carrier mobility resulting in shorter base transit time and has better etching selectivity with respect to InP. Some advanced III–V HBT designs are listed in Tab. 1.

Table 1. Examples of advanced HBT structures.

Structure [E/B/C]	f_T [GHz]	f_{max} [GHz]	Institution
GaInP/InGaAs/InP	100	150	OMMIC – Philips (France)
InP/GaAsSb/InP	> 300	> 300	Simon Frazer University (Canada)
AlInAs/GaAsSb/InP	160	300	UCSB (U.S.A.)

The most advanced structures are made using the so-called transferred substrate transistor [8], [9] where the emitter and collector are etched to form mesas (Fig. 3). This approach decreases the collector-base junction capacitance and allows minimising other parasitics. The recently introduced HBT structures would eventually reach f_{max} of 1.5 THz [8].

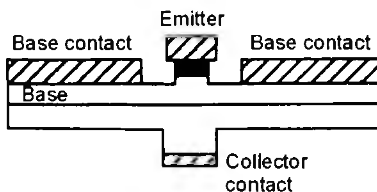

Fig. 3. Transferred substrate InP HBT schematics [8].

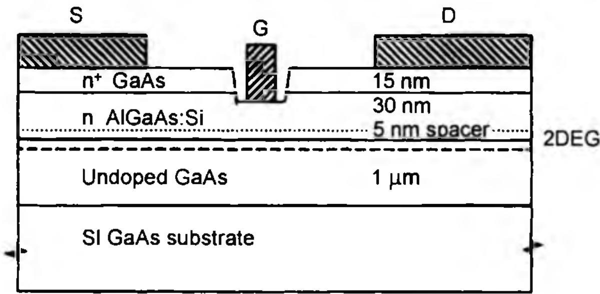

Fig. 4. Schematic cross-section of an AlGaAs/GaAs HEMT.

The III–V HEMT devices usually work in the communication equipment as an input stage, low noise amplifiers (LNA) or in the output stage as power amplifiers (PA), also in the optical communication photoreceiver modules [10]. In the HEMT development there is a continuous effort to lower the cost of substrates (InP) which determines the cost of a single device. The problem of maximum performance for a minimum cost here is particularly underlined. Maximum performance means high density of 2 DEG and high electron velocity/mobility. The design history of HEMTs started with AlGaAs/GaAs heterostructure with 2 DEG channel in the undoped GaAs (see Fig. 4), and has continued with InGaAs $In_{0.3}Ga_{0.7}As/GaAs$ pseudomorphic (strained) heterostructure (PHEMT) and $In_{0.53}Ga_{0.47}As/InP$ lattice matched structure (LMHEMT). The substrate cost for the last one is about $1000 per a 4 inch InP wafer, as compared to $400 for a 6 inch GaAs wafer. Thus, a new design, the so-called metamorphic (MHEMT), goes back to GaAs substrate and utilises a quaternary AlGaInAs metamorphic buffer layer with graded composition to compensate lattice mismatch between the active layer and the substrate. Some examples of the advanced HEMT structures reported at the 13th Conference on Indium Phosphide and Related Materials, 2001 in Nara, Japan [11] are listed in Tab. 2.

T a b l e 2. Examples of advanced HEMT structures.

FET type	Structure	L_g [nm]	f_T [GHz]	f_{max} [GHz]	Institution
PHEMT	InGaAs/InAlAs/InP	70	300	190	TRW (U.S.A.)
LM HEMT	InAlAs/InGaAs/InP	130	210	235	Raytheon (U.S.A.)
LM HEMT	InAlAs/InGaAs/InP	25	396	—	Fujitsu (Japan)
MHEMT	InP/InGaAs/AlInAs/GaAs	—	180	300	University of Ulm (Germany)
MHEMT	InGaAs/AlInAs/GaAs	150	—	450	Fraunhofer Inst. (Germany)

In our Semiconductor Devices Laboratory AlGaAs/GaAs epitaxial structures with 2 DEG have been grown by metal-organic vapour phase epitaxy (MOVPE). The epitaxial structures were processed to fabricate HEMT devices. The measured output

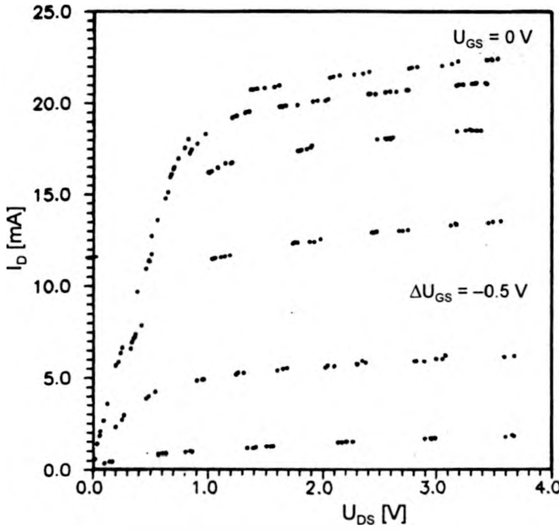

Fig. 5. Output current-voltage characteristics of the fabricated AlGaAs/GaAs HEMT.

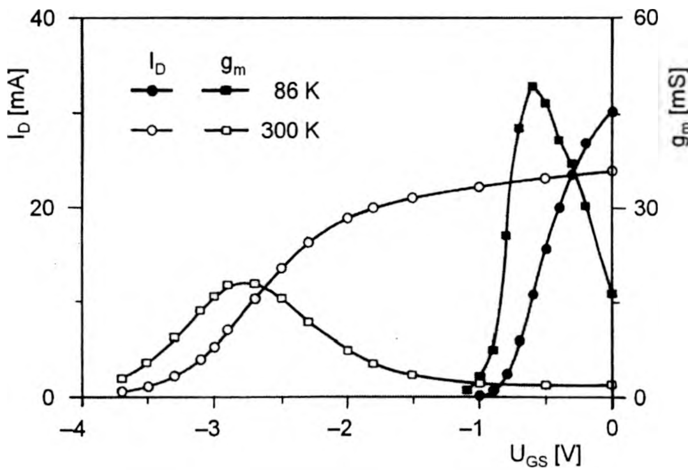

Fig. 6. Small signal transconductance dependence on the gate-source voltage of the fabricated HEMT measured at two temperatures.

current-voltage characteristics are presented in Fig. 5 and the small signal transconductance dependence on the gate voltage bias is shown in Fig. 6.

4. III–N devices

The group III nitrides, Ga(In,Al)N, are the most promising materials for high temperature operating devices. On the contrary, earlier designed SiC transistors are still at the laboratory research stage due to prohibitive high cost of the material ($5000

per 2 inch wafer) and lack of heterostructure capability. Only recently reports on commercial power SiC metal semiconductor field effect transistor – MESFETs (Cree CRF 20010) that deliver 10 W at 3.5 GHz have been published [12]. The AlGaN/GaN system owing to the large bandgap value, piezoelectric properties, high electron saturation velocity and large conduction band offset is attractive for HFETs. Due to large breakdown electric field, GaN is most suitable for high power application for devices operating with large voltage swing. In Figure 7 the comparison of the impact ionisation coefficient values for typical semiconductors is shown. Large breakdown field would allow also for much more intense lateral scaling of GaN device geometry. The gate length L_g, below 10 nm could be obtained for future GaN/sapphire VLSI applications, whereas that would be practically impossible for GaAs and Si devices due to excessive leakage current and breakdown [13]. Variety of GaN devices, including HBT, MOSFET, MODFET, HFET have been reported in papers [15]–[20], among them the most developed structures are HFETs capable to operate at frequencies above 100 GHz [12].

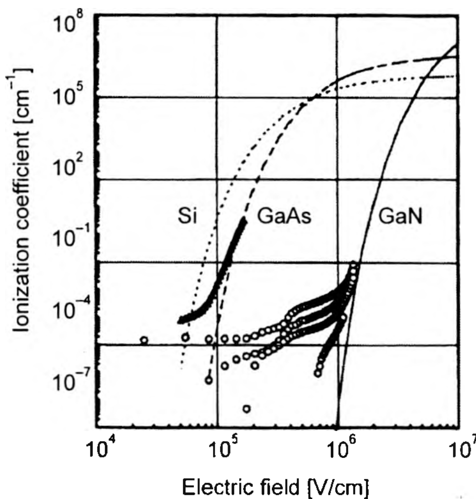

Fig. 7. Impact ionisation coefficient *vs.* the electric field for different materials [14].

Despite recent progress in HFET design, the heterostructure growth process and device fabrication techniques are still far from being optimised. For HFET fabrication, beside the high quality of a wide bandgap AlGaN layer, high carrier mobility in the GaN layer is required. Sapphire as a basic substrate for GaN growth is used, except for high power devices where SiC substrate is preferred [19]. Because of the large lattice mismatch between GaN and sapphire the active layers must be grown on thick (> 1 μm), highly resistive GaN buffer layers with low density of defects. Some examples of the state-of-the-art power devices include a "flip-chip" HFET bonded to AlN substrate of Cree Lighting with a gate width of 8 mm and gate length of 0.5 μm with $f_T = 30$ GHz, and $f_{max} = 60–100$ GHz. It performs with 50 W pulse power at

6 GHz and a Hughes Laboratories (U.S.A.) GaN/SiC substrate HFET with a gate width of 4 mm and gate length of 0.5 μm performing with cw power of 22 W at 9 GHz.

Our research on III–N materials includes studies of the epitaxial growth and design and fabrication of microelectronic and optoelectronic devices such as Schottky diodes, HFETs, UV MSM (metal–semiconductor–metal) photodetectors. Careful optimisation of the MOVPE process performed in our laboratory allowed decreasing electron concentration in undoped GaN layers to the level of 10^{16} cm^{-3}. $Al_xGa_{1-x}N$ layers with $0.02 \leq x \leq 0.22$ were grown on a 2 μm thick undoped high temperature GaN buffer deposited on sapphire substrate [21].

Using the obtained AlGaN/GaN heterostructures, test structures of HFET devices have been designed and fabricated [22]. In the design, a circular contact electrode topology has been proposed to avoid a cumbersome mesa etching process. In this case, the gate electrode is almost completely surrounded by the drain electrode; thus the parasitic shunt drain current is eliminated. The HFET topology, along with the circular transmission line method (CTLM test structures) is shown in Fig. 8. The gate length was 3 μm and the drain-gate and source-gate separation was 2 μm.

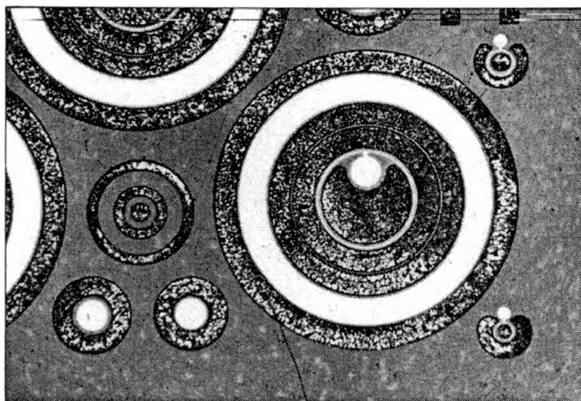

Fig. 8. Fabricated AlGaN/GaN HFET of a circular topology and the test structures.

The drain and source ohmic contacts were made using Ti/Al/Ni/Au metallization deposited in a single UHV process. After the lift-off, the wafer was annealed in nitrogen ambient. To obtain good contact surface morphology a second metallization of Ti/Au was applied. The gate Schottky contact has been made of Pt/Au metallization deposited by e-beam technique and the lift-off process. The calculated Schottky barrier potential was 0.8 V, which matched the expected value for Pt.

The measured *I–V* characteristics of the first GaN HFET device are presented in Fig. 9. The saturated drain current was 25 mA for the total gate width of 300 μm. The gate pinch-off voltage was 4 V. The parallel leakage current below the pinch off, caused probably by the parasitic channel in the GaN buffer, was observed. The small signal transconductance of the HFET was 8 mS. This made the total characteristic transconductance reach 27 mS/mm. An improved AlGaN/GaN on sapphire

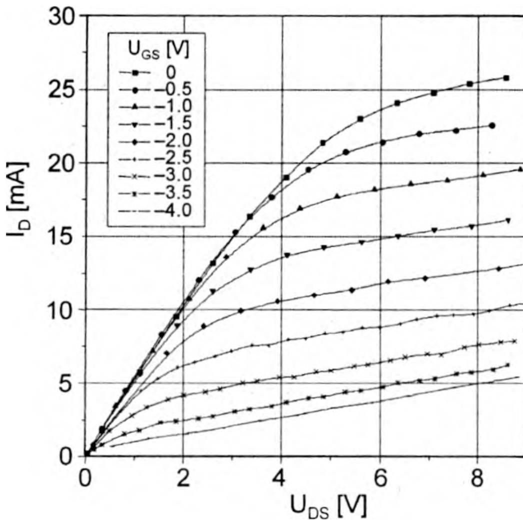

Fig. 9. Measured output characteristics (U_{GS} from 0 V to –4 V, step 0.5 V) of the first HFET fabricated in the laboratory at the Wrocław University of Technology.

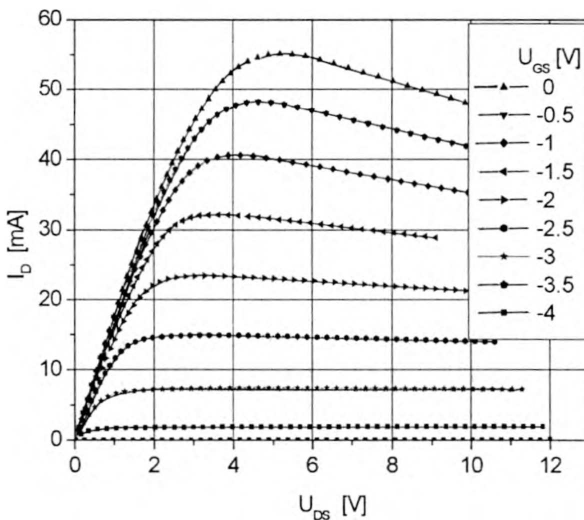

Fig. 10. Measured output characteristics (U_{GS} from 0 V to –4 V, step 0.5 V) of the recently fabricated HFET in the laboratory at the Wrocław University of Technology.

heterostructure was used to fabricate the HFET according to the device processing scheme described above. The resulting *I–V* characteristics are presented in Fig. 10. The measured transconductance value has doubled comparing to the first HFET and was 18 mS and the characteristic transconductance was 60 mS/mm. The preliminary measurements of high frequency parameters revealed f_T close to 1 GHz, which is a quite good result for the 3 μm gate length used in this design.

5. Future trends

An advanced research program for semiconductor devices devoted to ultra fast electronics has been established recently in the USA. It covers antimonide based compound semiconductors, (the so-called ABCS group: GaSb, AlSb, InAs *etc.*), which are characterised by closely matched lattice constants (0.61 nm ± 1%) and the possibility of energy gap tailoring within the range of 0.3–1.6 eV. That would allow designing variety of quantum well heterostructure devices with extremely high mobility of carriers, and covering broad IR spectrum for optoelectronics. The short-term goals are to obtain suitable semi-insulating substrates with low density of defects and to demonstrate device operation at frequencies above 100 GHz. The ultimate goal is to fabricate fast switching integrated circuits with very low dissipating power.

Another advanced research is devoted to introducing organic semiconductors to fast nanoscale device fabrication. A widespread application of organic semiconductors in LED's and thin film transistors market has already been observed [23]. For very high frequency devices and circuits possible materials include carbon nanotubes, semiconductor nanowires, small organic molecules and biomolecules. During the last decade IBM and Delft University developed first devices which demonstrated single molecule operation.

Strong research pressure is seen also in the area of spintronic quantum devices. Control of electron spin orientation in ferromagnetics and electron tunnelling through thin barriers is essential for the device operation. This group of active devices, now under laboratory study, includes resonant tunnelling transistor, ballistic effect spin FET or optically controlled spin FET [24].

6. Conclusions

From the historical review of the transistor development it is seen that basic inventions and fundamental description of principles of device operation have been made some 40–50 years ago. The progress has been possible mainly due to mastering of the device design rules and refining materials technology. Silicon remains and a long time will be the basic material due to excellent and "well-behaved" parameters easily described by formulas. Development of SiGe alloys allowed extending operation of Si devices and integrated circuits into high frequency region.

For the ultra high frequency communication and optoelectronic application III–V material devices are the solution with a new group of antimonide based materials emerging. For power and high temperature devices, GaN looks undefeated and seems to win over SiC, due to the expected material cost lowering of the former.

New devices based on ferromagnetics or organic molecules, although well described theoretically, are still in the preliminary laboratory research stage (with frequently published astonishing results) and their wide application is not expected for the next 10–20 years.

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