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All-optical parity generator and checker circuit employing semiconductor optical amplifier-based Mach–Zehnder interferometers

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Checking the parity of the data signal during transmission and reception is one way to ensure errorless transmission of data. In this communication the authors propose a method to implement an all-optical parity generator and checker using semiconductor optical amplifier-based Mach–Zehnder interferometers. The scheme, able to process input signals at the same wavelength, is characterized using return-to-zero modulated signals at 10 Gb/s. Correct logic bit sequences and clear open eye patterns with extinction ratios exceeding 10 dB are achieved. Simple structure and potential for integration make this architecture an interesting approach in photonic computing and optical signal processing.

Keywords: optical computing, semiconductor optical amplifier (SOA), semiconductor optical amplifier -based Mach–Zehnder interferometer (SOA-MZI), XOR gate, parity generator, parity checker.

1. Introduction

In order to meet the ever-increasing demand of data communication for future optical networks, high speed digital processing is required. Photonics signal elaboration at the optical layer is attractive to perform various computational functionalities, such as packet buffering, bit-length conversions, header processing, switching, retiming, reshaping, data encoding and encryption, and overcoming all the speed electronics limitations [1].

As it is well-known, in electronic digital communication, parity check is one of the most widely used binary manipulations and is attached to a binary word before transmission of the data so that the receiver has the ability to verify the integrity of the recovered digital data [2]. In long haul communication systems, there is great chance of signal degradation due to lossy fiber or lossy medium. If a specific channel fails to give the required intensity, then optical circuit considers it 0 instead of 1. This can lead to major errors. Thus an optical parity generator and checker circuits play an important role to identify these problems [3].

An all-optical parity checker employing terahertz optical asymmetric demultiplexers (TOAD) and using bit differential delay technique has been reported by

POUSTIE *et al*. [4]. Many designs for a parity checker or checker with generator have been proposed using a nonlinear material based intensity encoding [5], polarization encoded light signal [6], frequency encoded light signal [7], a micro-ring resonator [8], cross-gain modulation (XGM) effect in semiconductor optical amplifier (SOA) [2], quantum dot semiconductor optical amplifier (QD-SOA) based Mach–Zehnder interferometer (MZI) [9], and an electro-optic effect in lithium niobate ($LiNbO_3$) based MZI [3, 10].

In the parity checker circuits employing a bit differential delay technique, there is a round trip delay which increases the time-of-flight (TOF) latency in the design [2]. The operation of nonlinear material based intensity encoding circuit largely depends on the intensity of optical beams. Intensity encoded and polarization encoded methods have restricted usability as it is very difficult to maintain threshold intensities of the intensity encoded data and the specific states of polarization of the polarization encoded data in long haul communication system. Frequency encoded parity checkers are free from light intensity and polarization problems but they need a number of components for their implementation, thus making these circuits more complex and bigger in size [3].

The operation speed of the parity checker that is based on XGM effect in a SOA depends on the carrier recovery lifetime in the active region of the SOA [2]. Lithium niobate based devices have disadvantages of high insertion loss, high crosstalk and limited scalability. It is challenging to realize densely integrated photonic circuits on the $LiNbO_3$ platform [11]. Interferometric gates based on MZI and using SOA as a nonlinear element have attracted lots of interest due to its extremely high operational speed and tremendous potential for integration with a wide variety of active and passive components as well as its low power consumption and high stability [12]. In [9], data integrity verification is obtained by the XOR gates employing QD-SOA based MZI. In order to perform the XOR function, a clock stream held continuously to logical 1 is applied to the XOR gate along with the two input data streams.

In this work we present a simple, polarization independent and potentially integrable scheme for realization of an all-optical even parity generator and checker using SOA-based MZIs. The scheme, able to process input signals at the same wavelength, is characterized using return-to-zero (RZ) modulated signals at 10 Gb/s. Correct logic bit sequences and clear open eye patterns with extinction ratios exceeding 10 dB can be observed at the output.

2. Operating principle

In network transportation, either electrical or optical transfer, security is one of the most important issues. There are many techniques which have been proposed to reach safe communication. One of the common methods is using parity bits in data packets. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message, including the parity bit, is transmitted and then checked

at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator. The circuit that checks the parity in the receiver is called a parity checker.

Table 1 presents the truth table of a three-bit even parity generator, showing that the parity output P is in the logic state 1 only when input contains odd number of 1's. Otherwise, it is in logic state 0. The parity error check (PEC) output of the parity checker will be in the logic state 1 if an error occurs, that is, if the four bits received (including the parity bit) have an odd number of 1's – see Table 2.

T a b l e. 1. Truth table of parity generator.

Three-bit message			Parity bit
A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

T a b l e. 2. Truth table of parity checker.

Four bits received				Parity error check (PEC)
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

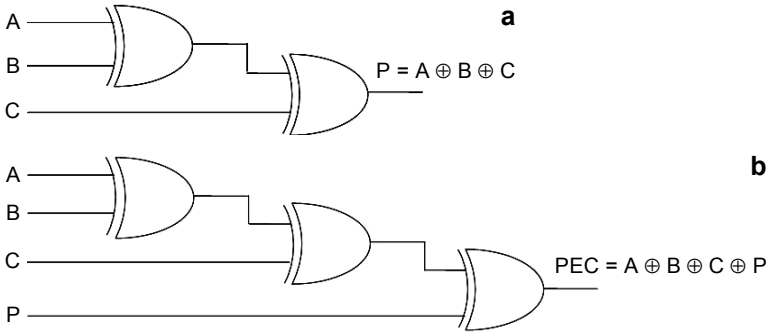

Fig. 1. Conventional layout of three-bit even parity circuits: parity generator (**a**), and parity checker (**b**).

In electronic domain, these circuits are fabricated with cascaded XOR gates. Figures 1**a** and 1**b** reveal the structure of three-bit even parity generator and checker, respectively. The two input data bits A and B are applied to the first XOR gate of the parity generator. The output of this XOR operation is XORed again with input bit C to produce the parity output. Parity checker circuit comprises three XOR gates to produce the PEC output.

The proposed architecture for the all-optical parity generator and checker is shown in Fig. 2. The XOR gates are realized using SOA-based MZI with the same SOA placed in each of the arms [13]. The wavelengths of three continuous-wave (CW) beams generated by laser diodes are 1553.32 nm (λ_1), 1550.92 nm (λ_2) and 1551.72 nm (λ_3), respectively.

Two optical input data signals A and B at a wavelength of 1553.32 nm (λ_1) and a CW control signal at wavelength of 1550.92 nm (λ_2) are applied to the XOR gate 1 of the parity generator. A Gaussian tunable optical bandpass filter (OBF 1) of 0.4-nm bandwidth is used to filter out the A XOR B signal at a wavelength of 1550.92 nm (λ_2). The output of the XOR gate 1 and input data signal C (1553.32 nm (λ_1)) act as input signals to XOR gate 2. A CW signal at a wavelength of 1551.72 nm (λ_3) is applied as a control signal to this XOR gate. OBF 2 is used to filter the P output at a wavelength of 1551.72 nm (λ_3).

Parity checker is identical with the parity generator except for the additional XOR gate (XOR gate 3). It accepts the fourth input as a received parity input and generates the PEC output at a wavelength of 1553.32 nm (λ_1) (input data signal wavelength). Optical amplifiers and variable optical attenuators (VOAs) are used at various stages of the setup to adjust the power levels of the signals.

3. Results

The numerical evaluations for a proof of the principle of operation are based on an experimentally validated simulation model, confirming that escalation of processing

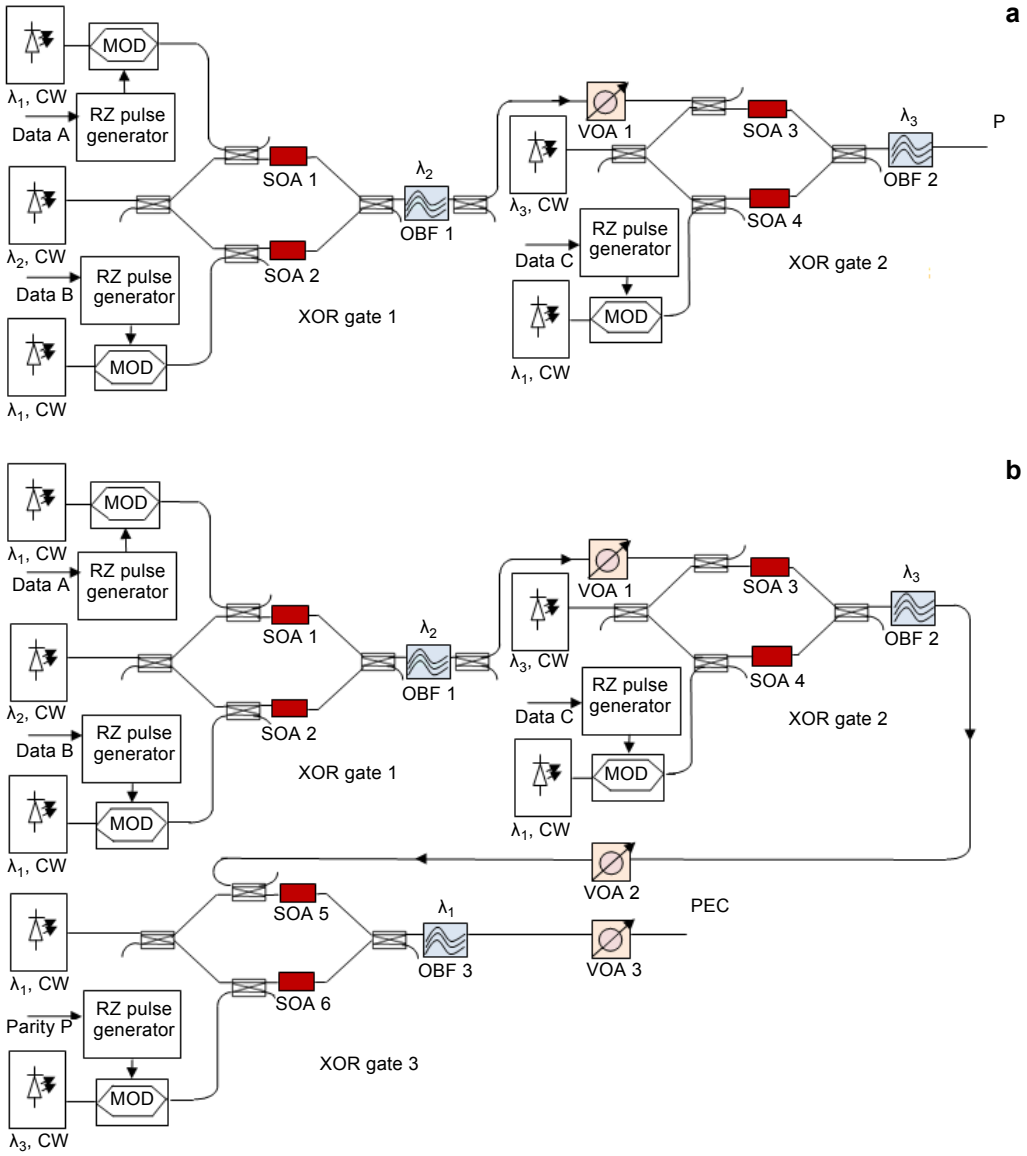

Fig. 2. Schematic configuration of all-optical parity generator (**a**) and parity checker (**b**).

speed to multi-Gb/s levels is feasible. The time-domain simulation model relies on the transfer matrix method (TMM) [14, 15].

Each SOA is identical and characterized by a length of 900 μm, an active-layer width of 1.2 μm, an active-layer thickness of 0.1 μm, a confinement factor of 0.2, a bias current of 300 mA, an active-region refractive index of 3.2, a cladding refractive index

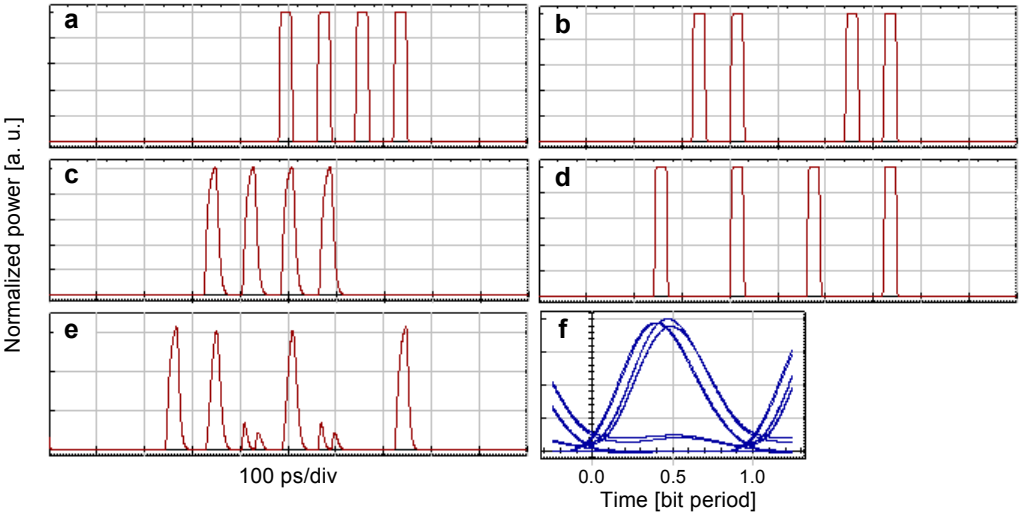

Fig. 3. Time-domain simulation of the proposed all-optical parity generator: input data signal A (**a**), input data signal B (**b**), XOR gate 1 output (A XOR B) (**c**), input data signal C (**d**), parity output P (**e**), and the corresponding eye diagram (**f**).

of 3.0, and a carrier lifetime of 40 ps. To our knowledge, the only assumption we did is neglecting polarization issues. As it is well-known, the polarization states of signals at the inputs of an SOA-MZI must be carefully controlled to achieve optimum performance. In a practical setup, a slight deviation of the optimum polarization states of the input signals would give rise to a reduction in the output power and device efficiency or performance, but there is no influence on the operation of the circuit.

A simulation timing diagram of the all-optical parity generator is shown in Fig. 3. The input signals A, B, and C are RZ modulated with a duty cycle of 33% at 10 Gb/s. Two optical input data signals A and B at a wavelength of 1553.32 nm (λ_1) are applied to XOR gate 1, which is realized using an SOA-based MZI. A CW control signal at wavelength 1550.92 nm (λ_2) with a power of 0.5 mW acts as a third input to the SOA-MZI. The input data signals A and B with a peak power of 0.5 mW before entering the XOR gate 1 are shown in Figs. 3**a** and 3**b**, respectively. XOR gate 1 output at a wavelength of 1550.92 nm (λ_2) is shown in Fig. 3**c**.

The simulation results of Fig. 3**c** show a high extinction ratio (values higher than 15 dB) for the signal at the output of XOR gate 1. The main reason for this high performance is that the "zero/off" level is almost perfect due to the destructive interference of the bias power and the two data signal pulses in their respective SOAs at the output of the SOA-MZI during the period of occurrence of 3rd and 4th input optical data signal pulses.

Figure 3**d** shows the input data signal C at a wavelength of 1553.32 nm (λ_1) with a peak power of 0.5 mW. The input data signal C and output of XOR gate 1 act as input

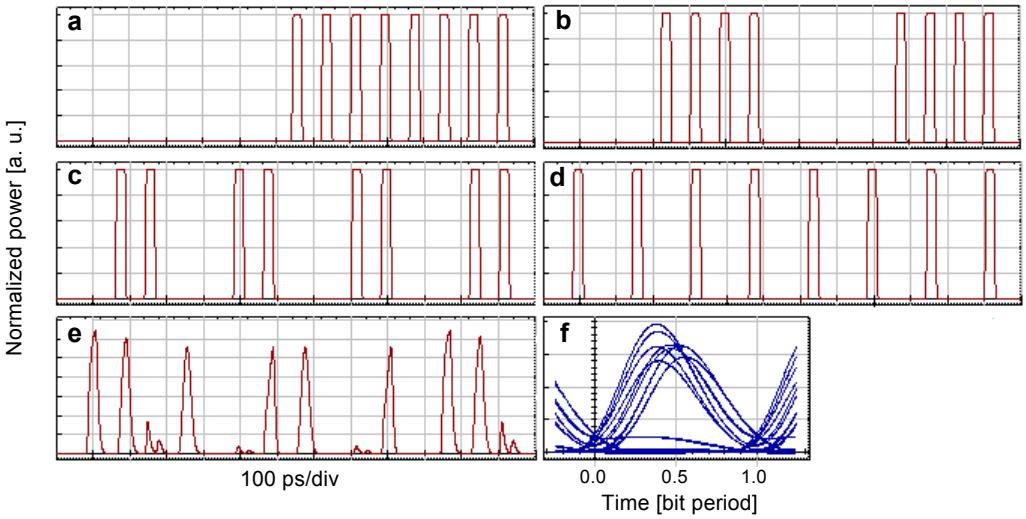

Fig. 4. Input and output waveforms of the proposed all-optical parity checker: input data signal A (**a**), input data signal B (**b**), input data signal C (**c**), parity input signal P (**d**), PEC output (**e**), and the corresponding eye diagram (**f**).

signals to XOR gate 2, which uses a CW signal at a wavelength of 1551.72 nm (λ_3) as the control signal. The parity output signal P generated from the logic XOR operation at a wavelength of 1551.72 nm (λ_3) and its corresponding eye diagram are shown in Figs. 3**e** and 3**f**, respectively.

We observe some small residual pulses in the output, where ideally they should not appear. The extinction ratio of the parity output signal P was found to be 11.7 dB. The reasons for the lower performance of the signal were noise accumulation and the lower extinction ratio of the pulses used for switching XOR gate 2.

Input and output waveforms of the parity checker are shown in Fig. 4. The input data signals A, B and C at a wavelength of 1553.32 nm (λ_1) with a peak power of 0.5 mW are shown in Figs. 4**a**, 4**b** and 4**c**, respectively. XOR gate 1 and XOR gate 2 of the parity checker are implemented in an identical manner with that of the parity generator. Figure 4**d** shows the input parity signal P at a wavelength of 1551.72 nm (λ_3) with a peak power of 0.5 mW. The input parity signal P and output of XOR gate 2 act as input signals to XOR gate 3, which uses a CW signal at a wavelength of 1553.32 nm (λ_1) as the control signal. The PEC output signal generated from the logic XOR operation at a wavelength of 1553.32 nm (λ_1) (input data signal wavelength) and its corresponding eye diagram are shown in Figs. 4**e** and 4**f**, respectively.

The extinction ratio of the PEC output signal was found to be 10.4 dB. Figure 5 shows the measured extinction ratios and eye opening factors at the outputs of all-optical parity generators and checkers. Extinction ratios obtained for A XOR B, P and PEC outputs are 15, 11.7 and 10.4 dB, respectively. Eye opening factors for the cor-

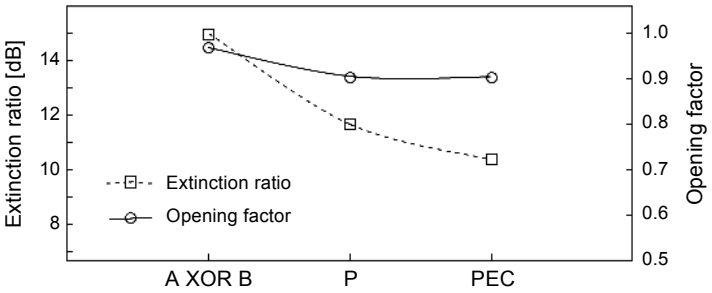

Fig. 5. Extinction ratios and opening factors of the output signals.

responding outputs are 0.97, 0.906 and 0.905, respectively. All extinction ratios exceed 10 dB, and the eye opening factors exceed 0.9.

4. Conclusion

We present a simple, polarization independent and potentially integrable scheme to realize an all-optical three-bit even parity generator and checker using SOA-based MZIs. The scheme is able to process the input signals at same or different wavelength, thus making it wavelength independent. Proof-of-principle operation is numerically evaluated at 10 Gb/s using return-to-zero data patterns. Wide and clear eye patterns for the different logic outputs with extinction ratios exceeding 10 dB are achieved. As parity checking is an essential component in any communication system and it ensures the correctness of sending data at the receiving point, so the proposed all-optical system can exhibit a strong application in optical communication as well as in computation.

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